HIGH-SPEED POSITION DETECTOR USING NEW ROW-PARALLEL ARCHITECTURE FOR FAST COLLISION PREVENTION SYSTEM

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ABSTRACT

A high-speed position detector has wide variety of application fields such as real-time range finding and high-speed visual feedback in robot vision. In this paper, a row-parallel sensor architecture for high-speed position detection is presented. The edge of activated pixels is quickly detected by a row-parallel search circuit and its encoding cycles of N-pixel horizontal resolution are O(log N). The architecture keeps high-speed position detection in high pixel resolution. We have designed and fabricated the prototype position detector with a 128 × 16 pixel array in 0.35 μm CMOS process. The measurement results show it achieves high-speed detection of 450 ns. The high-speed position detection of the scanning sheet beam is demonstrated.

1. INTRODUCTION

A high-speed smart position sensor has wide variety of application fields such as real-time range finding, high-speed visual feedback in robot vision and so on. These applications require much higher speed of frame rate than the conventional imagers using serial readout and transmission. Therefore some smart sensors were proposed for high-speed position detection [1]–[6].

Fig.1 shows a fast collision prevention system with simple calculation, which is one of applications to require high-speed position detection. The scanning sheet beam activates pixels from the right to the left on the sensor plane. Two position detectors detect the edge of the activated pixels. The difference between x_R and x_L means the distance from the position detectors when the edge address of the left position detector is x_L and that of the right one is x_R. High-speed position detection realizes a fast and high-resolution collision prevention system. One forward scan with N-pixel horizontal resolution requires N frames of the scanning sheet beam. For example, 30k fps is required for real-time range finding with 1k-pixel horizontal resolution. The smart sensors [3]–[6] are useful for applications of high-speed position detection. These frame rates, however, are not enough to realize real-time or more high-speed range finding with high pixel resolution.

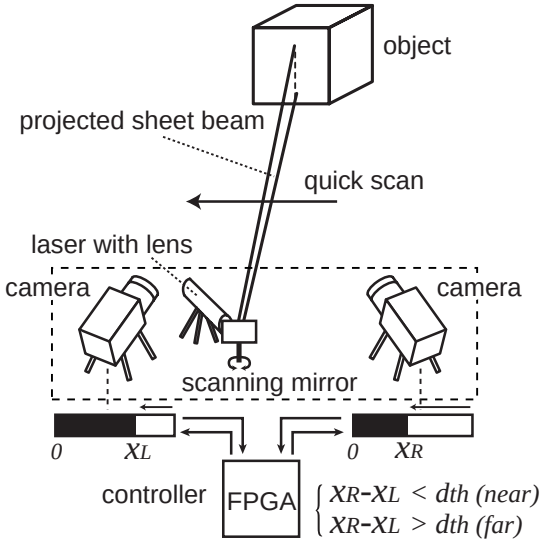

Figure 1: Fast Collision Prevention System.

In this paper, a row-parallel sensor architecture for high-speed position detection is presented. It achieves enough speed for real-time or more high-speed range finding with high pixel resolution. In this architecture, the edge of the activated pixels is quickly detected by a row-parallel search circuit and its encoding cycles of N-pixel horizontal resolution are O(log N). We have designed and successfully tested the prototype position detector with a 128 × 16 pixel array in 0.35 μm CMOS process.

2. ROW-PARALLEL ARCHITECTURE

In the position detection of a projected sheet beam, a sensor recognizes the pixels with strong incident intensity as the history of the scanning sheet beam as shown in Fig.2. Therefore it is important to quickly detect the position of the activated pixels in each row. The frontier line of the projected light provides enough information for triangulation-based range finding. Our architecture has a row-parallel search circuit for the edges of the activated pixels in each row, a row-parallel address encoder of O(log N) and a row-parallel processor to reduce data transmission.

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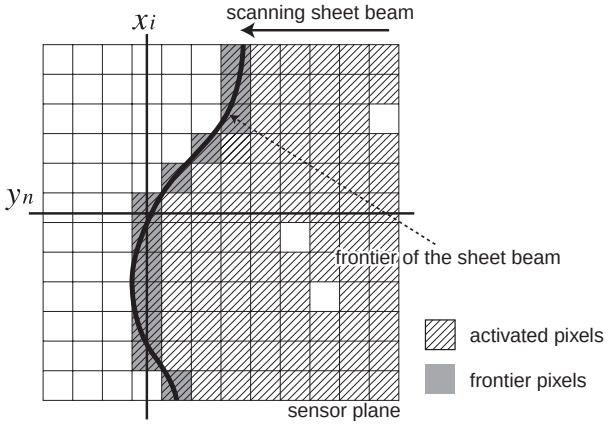

Figure 2: Captured image example of a sheet beam.

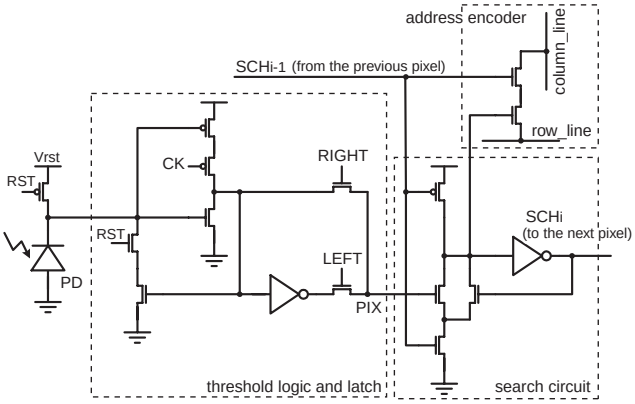

Figure 3: Pixel circuit.

2.1. Row-Parallel Search Circuit

Fig.3 shows a schematic of a pixel. It has a photodiode with a reset transistor, a threshold logic and latch circuit, a search circuit, and an address encoder. The latch circuit has an XOR circuit and can invert a pixel value *PIX*. At the search circuit, the search signal SCH_{i-1} from the previous pixel passes to the next pixel when the pixel value *PIX* is '1'. On the other hand, it stops when the pixel value *PIX* is '0'. Fig.4 shows a procedure of the row-parallel position search. Some pixels are activated by a strong incident light and they have a pixel value *PIX* of '0' as shown in Fig.4(a). The search signal SCH_0 is inputted to each row. It passes to the next pixel when the pixel value *PIX* is '1'. Thus the search signal stops at the left edge x_i of the activated pixels as shown in Fig.4(b). After a row-parallel encoding mentioned later, the pixel values *PIX* are inverted and the search signal starts again. It stops again at the next of the right edge x_j. The positions of the second and more activated pixels are detectable by the iteration of *PIX* inversions. It means that it is applicable to applications with a complex-shaped target object and/or multiple projected lights.

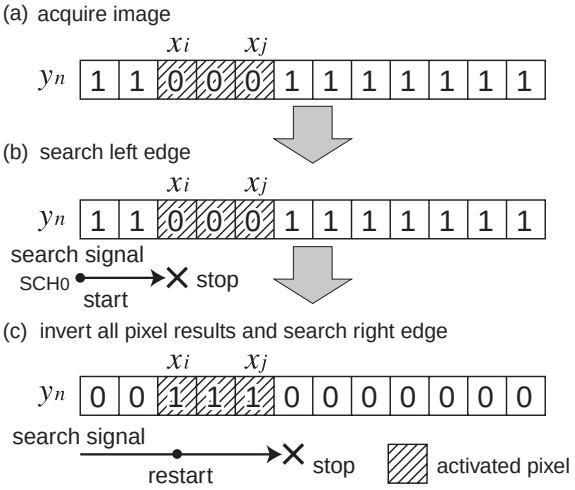

Figure 4: Procedure of row-parallel position search.

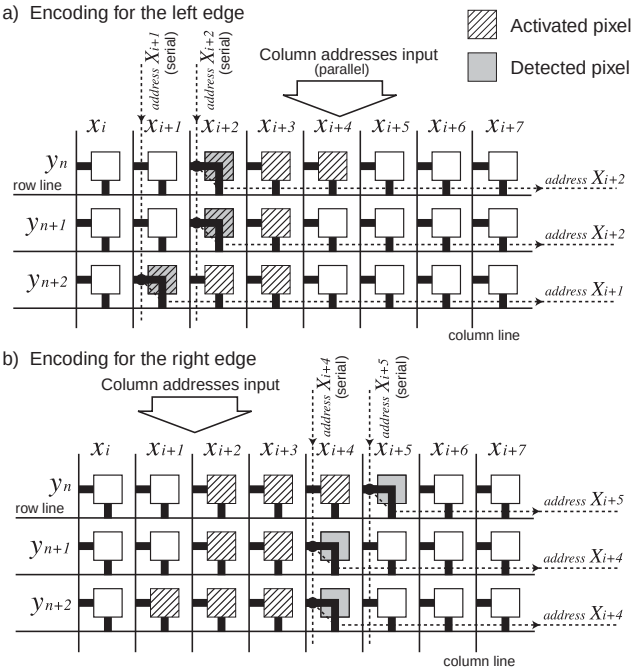

Figure 5: Method of row-parallel address encoding.

2.2. Row-Parallel Address Encoding

The address encoder of the pixel circuit consists of only 2 pass transistors as shown in Fig.3. At the detected pixel of each row, the column line is connected to the row line through the pass transistors as shown in Fig.5. Then, the serial-bit-streamed column address is inputted to each column line in parallel. Therefore the encoding cycles are O(log N) at N-pixel horizontal resolution. The compact circuit implementation and the high-speed row-parallel encoding realize high-speed position detection in high pixel resolution.

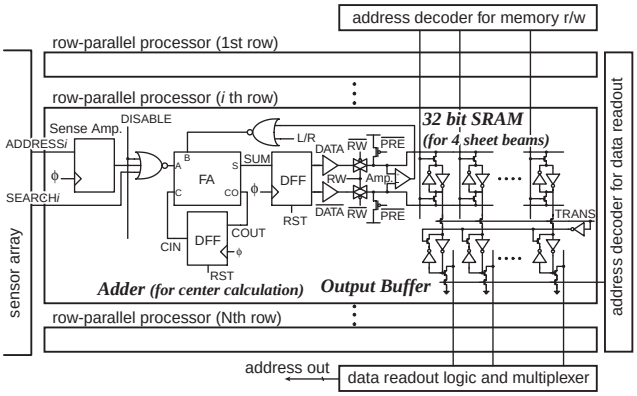

Figure 6: Structure of row-parallel processor.

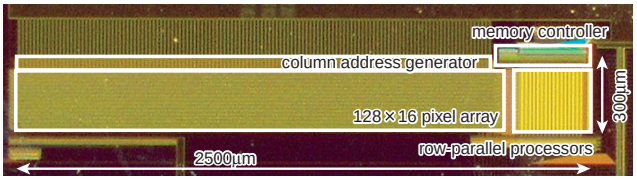

Figure 7: Chip microphotograph.

2.3. Row-Parallel Processor

The photo detector has a row-parallel processor as shown in Fig.6. It consists of a latch sense amplifier to get the address data, a full adder, random access memories with a read/write circuit, output buffers for pipe-lined data readout, and some control logics. The row-parallel address encoding can acquire the addresses of x_i and $x_j + 1$ when the edges of the activated pixels are x_i and x_j. The processor calculates the center position of the detected pixels and reduces data transmission. And also it realizes to get the positions of multiple sheet beams in one frame. The row-parallel processor can be extended to deal with another data processing. For example, multiple samplings per frame can be realized for high sub-pixel accuracy when a timing memory and its control logics are implemented.

3. CHIP IMPLEMENTATION

We designed and fabricated a prototype position detector in 0.35 μm CMOS process[1]. Fig.7 shows a microphotograph of the fabricated chip. It consists of a 128×16 pixel array, a column address generator, row-parallel processors with 32 bit SRAM per row and a memory controller. The pixel circuit has 1 photo diode and 18 transistors in 16.25 μm $\times$ 16.25 μm pixel area with 20.15 % fill factor.

[1]The VLSI chip in this study has been fabricated through VLSI Design and Education Center (VDEC) in collaboration with Rohm Corp. and Toppan Printing Corp.

Table 1: Specifications of the prototype chip.

Process	0.35 μm CMOS 3-metal 1-poly-Si
Sensor size	2.5 mm $\times$ 0.3 mm
# pixels	128×16 pixels
Pixel size	16.25 μm $\times$ 16.25 μm
# trans. / pixel	18 transistors
Fill factor	20.15 %

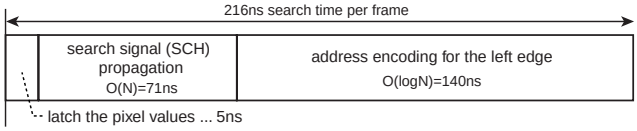

Figure 8: Simulated search time per frame for position detection of the fabricated chip.

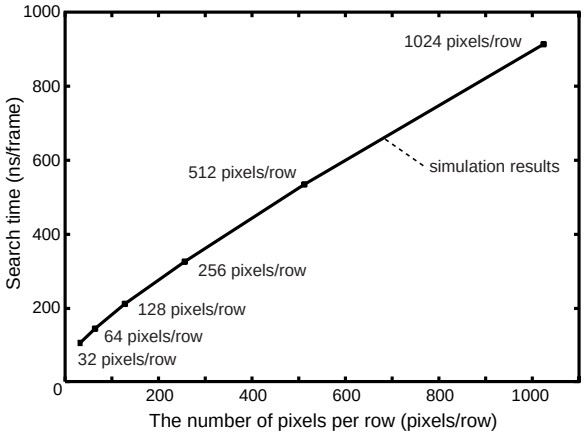

Figure 9: Search time in high pixel resolution.

4. PERFORMANCE EVALUATION

Fig.8 shows search time per frame for position detection simulated by HSPICE. The maximum propagation delay of the search signal is 71 ns and the 7-bit address encoding for 128 columns takes 140 ns. The total search time to get the position of the left edge of the activated pixels is 216 ns per frame. In a single sampling per frame, the frame interval is a total of the integration time of incident light and the search time for the left and right edges. The frame interval, however, is only the search time for the left edge in multi samplings per frame. That is, the sensor detects the frontier positions of the scanning sheet beam at each time during the integration of incident light. The present architecture achieves 918 ns search time per frame at 1024-pixel horizontal resolution. Generally real-time range finding of 1024×1024 pixels requires 32.5 μs search time per frame. The present architecture realizes enough speed not only for real-time range finding but also for beyond-real-time range finding and visual feedback.

Table 2: Performance comparisons.

	frame rate	# pixels
Our detector (single-sampling)	32.2k fps	128×16
	(31.4k fps)	1024×1024
Our detector (multi-sampling)	2.22M fps	128×16
	(1.09M fps)	1024×1024
Brajovic et al. [4]	6.4k fps	32×64
Sugiyama et al. [6]	3.3k fps	320×240
Required fps for real time	30.7k fps	1024×1024

Frame rates in parentheses are simulation results.

5. MEASUREMENT RESULTS

The measurement system of the fabricated chip has been developed as shown in Fig.1. In the system, the position detector and a scanning mirror are controlled by FPGA and the acquired position data are transferred to a PC. The FPGA was operated at 80 MHz due to the limitation of the testing equipment. The search time was 450 ns per frame and the integration time of incident light was 30 μs at V_{rst} = 1.4 V. Fig.10 shows the measurement results of the present position detector. Fig.10(a) shows the position of the left and right edges of the activated pixels. That is, the projected sheet beam is located between these edges on the sensor plane. The position detector has the processor to calculate the center position on the chip. Only the center address can be acquired to reduce data transmission as shown in Fig.10(b). Fig.10(b) shows sequentially captured positions of the scanning sheet beam of 2 kHz by single sampling per frame. It takes 30.9 μs per frame. It has 256 sub-pixel resolution due to the center calculation. Fig.10(c) shows the frontier positions of the scanning sheet beam. It takes 0.45 μs per frame. The results show the frame rate is 32.2k fps and 2.22M fps in a single sampling and multi samplings per frame respectively. The performance comparisons are shown in Table 2.

6. CONCLUSIONS

A row-parallel sensor architecture for high-speed position detection has been proposed. It has been designed and fabricated in 0.35 μm CMOS process and successfully tested. The prototype position detector has 128×16 pixels and it achieves 450 ns search time per frame. In the measurement system using multi samplings per frame, the high-speed position detection of a scanning sheet beam is realized at 2.22M fps. It is enough speed not only for real-time range finding but also for beyond-real-time range finding and visual feedback such as a fast collision prevention system. We have also shown its applicability to higher pixel resolution such as 1024×1024 pixels.

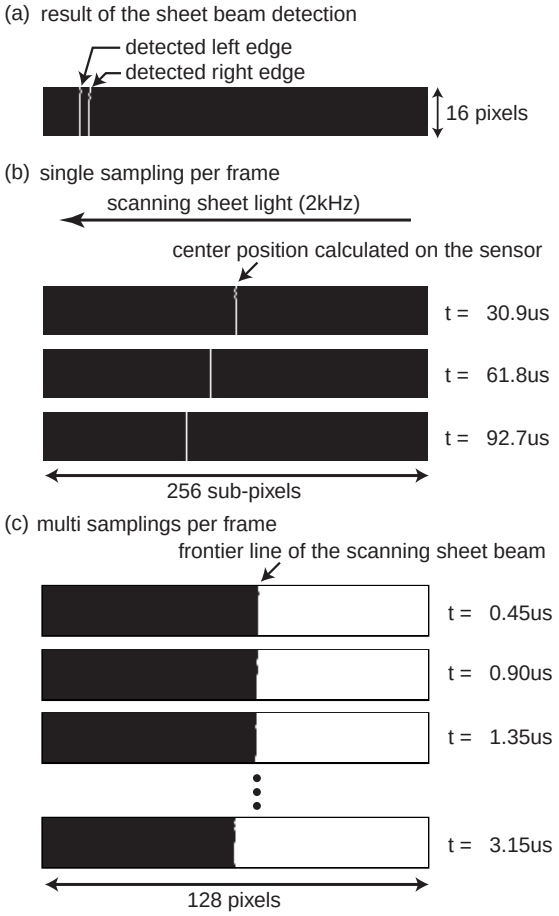

Figure 10: Measurement results.

7. REFERENCES

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